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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,977	12/08/2003	Belford T. Coursey	MI22-2459	2810
21567	7590	09/16/2005		
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			EXAMINER FENTY, JESSE A	
			ART UNIT 2815	PAPER NUMBER
DATE MAILED: 09/16/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/728,977

Applicant(s)

COURSEY, BELFORD T.

Examiner

Jesse A. Fenty

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 38-44 and 48-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 38-44 and 48-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 38, 42, 48, 51 and 54-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwok et al. (U.S. Patent No. 5,770,499).

In re claims 38 and 42, Kwok discloses a semiconductor device, comprising:

a semiconductor substrate (102);

word lines (104) received over the semiconductor substrate;

an insulative layer (170) received over the word lines, the digit lines, and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, an area peripheral to the well comprising memory peripheral circuitry area (182), the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the one well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base over the word lines;

and

peripheral circuitry within the peripheral circuitry area (column 6, lines 1-5)..

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peripheral circuitry within the peripheral circuitry area (column 6, lines 1-5).

In re claim 42, Kwok (esp. Figs. 3-20) discloses a semiconductor device, comprising:

a semiconductor substrate (102);

word lines (104) received over the semiconductor substrate;

digit lines (109) received over the word lines;

an insulative layer (170) received over the word lines, the digit lines, and the substrate, the insulative layer having at least a single well formed therein, the well comprising a base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, an area peripheral to the well comprising memory peripheral circuitry area (182), an oxygen diffusion barrier layer (172) received over said the well base;

a plurality of memory cell storage capacitors received within said single well over the word lines and the digit lines, the memory cell storage capacitors respectively comprising a storage node container which is received within the insulative layer through the oxygen diffusion barrier layer and through the well base; and

peripheral circuitry within the peripheral circuitry area (column 6, lines 1-5).

In re claim 48, Kwok discloses the device of claim 38, wherein the oxygen diffusion barrier layer received over the well base comprises silicon nitride (column 5, lines 59-60).

In re claim 51, Kwok discloses the device of claim 48, wherein the insulative layer (170) comprises silicon dioxide.

In re claims 54 and 55, Kwok discloses the devices of claims 38 and 42 respectively, wherein one of the storage node electrodes is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

In re claim 56, Kwok discloses the device of claim 42, wherein the base is substantially planar.

In re claim 57, Kwok discloses the device of claim 42, wherein the insulative layer is formed to have a substantially planar outermost surface, the memory cell storage capacitors respectively comprising an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

In re claim 58, Kwok discloses the device of claim 42, wherein the silicon nitride comprising oxygen diffusion barrier layer is received on the well base.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 39-41, 43, 44, 49, 50, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwok as applied to claim 38 above, and further in view of Tu (U.S. Patent No. 6,200,898 B1).

In re claims 39 and 43, Kwok discloses the device of claims 38 and 42 respectively, but does not expressly disclose the height of the storage node electrode being elevationally proximate the substantially planar outermost surface of the insulative layer. Tu (esp. Figs. 4, 7-9) discloses a well region within an upper insulating layer (14) wherein the storage node electrode (18) is elevationally proximate the substantially planar insulating layer. It would have been obvious for one skilled in the art at the time of the invention to use the capacitor structure as disclosed by Tu for the device of Kwok for the purpose, for example, of raising the height of the capacitor to produce a top level topography for the upper electrode more in line with the external circuitry (Tu; column 6, lines 5-8).

In re claims 40 and 44, Kwok discloses the devices of claims 38 and 42 respectively, wherein the insulative layer is formed to have a substantially planar outermost surface, but does not expressly disclose the storage node electrodes having topmost surfaces elevationally above the substantially planar outermost surface of the insulative layer by less than 50 angstroms. Tu (Fig. 4) discloses a similar tortuous surface area storage node device to that of Kwok wherein the storage node layer (18) rises above the insulating layer (14). Upon removal of this layer, Tu does not expressly disclose that the layer (18) is entirely swept clean from the surface of the insulating layer (14). Based on the knowledge of those skilled in the art, unless explicitly

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disclosed in the reference, one would expect that the removal of the layer (18) would leave behind a small residual layer on the order of five angstroms or less. Such a layer is an inherent by-product of the nature of semiconductor technology and would meet the limitation of the claim.

In re claim 41, Kwok discloses the device of claim 38, but does not expressly disclose the well base having a lowest point which is received at least 1000 angstroms above outermost tops of the digit lines. Tu disclose digit lines (9) at a distance greater than 8000 angstroms from the base well layer (Tu; column 4, lines 1-3). It would have been obvious for one skilled in the art at the time of the invention to separate the bit lines from the bottom of the well layer which supports the capacitor structure for the purpose, for example, of protecting the word lines from damage during the making of the capacitor regions.

In re claims 49, 50, 52 and 53, Kwok discloses the devices of claims 38 and 42 respectively, but does not expressly disclose the thickness of the silicon nitride layer (120). Tu discloses a similar silicon nitride layer (13) having a minimum thickness of 100 angstroms (column 4, lines 20-23). Tu discloses the range of claims 49 and 52 but does not expressly disclose the range comprising 50 to 70 angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made to decrease the thickness of the silicon nitride layer since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Decreasing the thickness of the silicon nitride layer would contribute to the overall goal

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of making the semiconductor device smaller, such that more devices could be configured per unit wafer.

Response to Arguments

1. Applicant's arguments filed 05/31/05 have been fully considered but they are not persuasive.

a. Regarding claim 38, Applicant argues that "no portion of Kwok et al.'s storage node containers 136 are received partially within an insulative layer 110 or 170."

i. However, as detailed in the Non-Final Office Action mailed 03/25/05 and the instant action, the storage node is the layer referred to as item (116). The item (116) is clearly partially within the insulation layer 110.

ii. Furthermore, the term "partially within" is taken to mean that one portion of the layer (116) is "partially within" the insulating layer and another portion of the layer (116) is partially without of the insulating layer. This portion is the portion that overflows onto the surface of the insulating layer (110).

b. Regarding claim 42, Applicant amends the claim to include an "oxygen diffusion barrier layer" which is not analogous to the capacitor dielectric.

iii. In the instant rejection, Examiner has shifted the interpretation of the reference from using the dielectric layer (120), to the more appropriate

etch stop layer (170), made of silicon nitride, which is analogous to applicant's new claim limitation.

c. Regarding claim 40, Applicant disagrees with Examiner's conclusion about residue being left over after chemical mechanical polishing ("CMP"). Applicant is directed to S. Wolf, Volume 2, pp. 238. Wolf teaches that residual oxide will be left on the surface of active areas after polishing. This is precisely the effect Examiner refers to in the instant and the previous Non-Final rejection. Wolf goes on to disclose that an additional process would be required to completely remove all of the residue, such as by additionally using etchback planarization.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

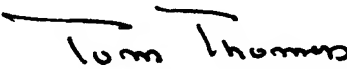
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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


TOM THOMAS
SUPERVISORY PATENT EXAMINER

Jesse A. Fenty
Examiner
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